INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT11Triple 3-input AND gate

Product specification
File under Integrated Circuits, IC06

December 1990





Triple 3-input AND gate

74HC/HCT11

FEATURES

· Output capability: standard

I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT11 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT11 provide the 3-input AND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYP	UNIT	
	PARAMETER	CONDITIONS	НС	нст	ONLI
t _{PHL} / t _{PLH}	propagation delay nA, nB, nC to nY	$C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$	10	11	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	18	20	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

f_i = input frequency in MHz

fo = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

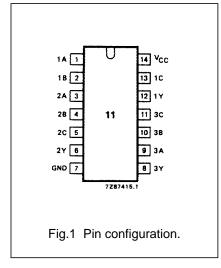
See "74HC/HCT/HCU/HCMOS Logic Package Information".

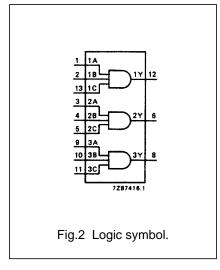
Triple 3-input AND gate

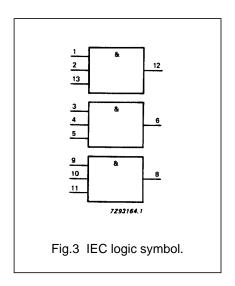
74HC/HCT11

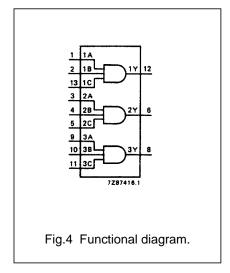
PIN DESCRIPTION

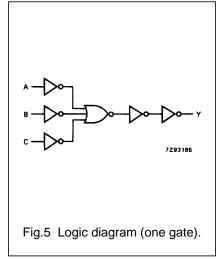
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
7	GND	ground (0 V)
12, 6, 8	1Y to 3Y	data outputs
13, 5, 11	1C to 3C	data inputs
14	V _{CC}	positive supply voltage











FUNCTION TABLE

	OUTPUT		
nA	nB	nC	nY
L	L	L	L
L	L	Н	L
L	Н	L	L
L	Н	Н	L
Н	L	L	L
Н	L	Н	L
Н	Н	L	L
Н	Н	Н	Н

Notes

H = HIGH voltage level
 L = LOW voltage level

Philips Semiconductors Product specification

Triple 3-input AND gate

74HC/HCT11

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

SYMBOL	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
		74HC									
		+25			-40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		(1)	
t _{PHL} / t _{PLH}	propagation delay		32	100		125		150	ns	2.0	Fig.6
	nA, nB, nC to nY		12	20		25		30		4.5	
			10	17		21		26		6.0	
t _{THL} / t _{TLH}	output transition		19	75		95		110	ns	2.0	Fig.6
	times		7	15		19		22		4.5	
			6	13		16		19		6.0	

Triple 3-input AND gate

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

'To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT						
nA, nB, nC	1.00						

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

SYMBOL	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
		74HCT									
		+25		-40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		(-,	
t _{PHL} / t _{PLH}	propagation delay nA, nB, nC to nY		16	24		30		36	ns	4.5	Fig.6
t _{THL} / t _{TLH}	output transition times		7	15		19		22	ns	4.5	Fig.6

AC WAVEFORMS

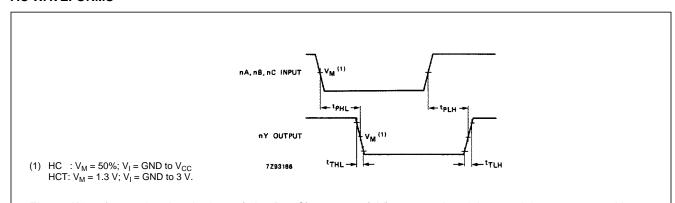


Fig.6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".